REMARKS

Claims 1-9 and 19-24 are pending in the present application. Claims 1, 19, and 23 are amended above. No new matter is added by the claim amendments. Entry is respectfully requested.

The Applicants note that the Office Action Summary does not indicate whether the drawings filed in the application are acceptable. Confirmation of their acceptability is respectfully requested.

The Applicants note with appreciation that the Office Action indicates at page 10 that claims 3-5, 7, 21-22 and 24 would be allowable if rewritten in independent form. The Applicants wish to defer submission of these claims, pending consideration of the present Amendment.

Claims 1, 6, 8-9, 19-20 and 23 stand rejected under 35 U.S.C. 103(a) as being anticipated by Suemura *et al.* (U.S. Patent No. 5,887,039 - hereinafter "Suemura") in view of Co, *et al.* (U.S. Patent No. 5,602,882 - hereinafter "Co). Claim 2 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Suemura in view of Co, and in further view of Sakamoto, *et al.* (U.S. Patent No. 6,557,110 - hereinafter "Sakamoto"). Reconsideration and removal of the rejections, and allowance of the claims, are respectfully requested.

In the present invention as claimed in amended independent claim 1, an optical transfer system includes a "receiver" that in turn includes a "receiver phase locked loop" that generates a "second plurality of non-overlapping clock signals of different respective phases" in response to a "received clock" included in the received optical signal. At least one of the non-overlapping clock signals is "in phase with the received clock."

In the present invention as claimed in amended independent claim 19, a data restoration and skew compensation unit in a receiver generates "first through n-th non-overlapped clock

signals in response to a clock signal received on a transmission channel." The unit includes a first latch unit that latches received serial data in response to the first through n-th non-overlapped clock signals of different respective phases that are generated in response to the received clock signal. At least one of the first through n-th non-overlapped clock signals is "in phase with the received clock signal."

In the present invention as claimed in amended independent claim 23, a method of restoring information data comprises generating first through n-th non-overlapped clock signals. Each clock signal has a predetermined offset and a different respective phase to prevent mutual overlapping, on the basis of a clock signal received via a transmission channel. At least one of the first through n-th non-overlapped clock signals is "in phase with the received clock signal".

Suemura discloses a method of transmitting parallel digital data in one or more channels that includes frame synchronization and skew compensation. The Office Action states at page 4, paragraph 1, and at page 7, paragraph 1, that Suemura fails to teach the generation of a plurality of non-overlapping clock signals of different phases in response to a clock signal. Co is cited in the Office Action at page 4, paragraph 2 and at page 7, paragraph 2 as teaching multi-phase clocks.

With regard to the rejection of independent claim 1, it is submitted that the combination of Suemura and Co fails to teach or suggest the present invention as claimed. In particular, the combination of Suemura and Co fails to teach or suggest the receiver generating a second plurality of non-overlapping clock signals of different respective phases "in response to a received clock". In Suemura, non-overlapping clock signals are not generated. In Co, the multiple-phase clock signals of Fig. 4 (element 32 of Fig. 3 of Suemura) are generated by a phase locked loop in response to the output of a 32 MHz external crystal oscillator, and not in response to a received clock signal. In view of this, it is further submitted that the combination of Suemura and Co fails to teach or suggest at least one of the non-overlapping clock signals being "in phase with the received clock," as claimed.

With regard to the rejection of independent claim 19, it is submitted that the combination of Suemura and Co fails to teach or suggest the present invention as claimed. In particular, the combination of Suemura and Co fails to teach or suggest a data restoration and skew compensation unit in a receiver that generates "first through n-th non-overlapped clock signals in response to a clock signal received on a transmission channel." In Suemura, non-overlapping clock signals are not generated. In Co, the multiple-phase clock signals of Fig. 4 (element 32 of Fig. 3 of Suemura) are generated by a phase locked loop in response to the output of a 32 MHz external crystal oscillator, and not in response to a clock signal received on a transmission channel. In addition, the combination of Suemura and Co fails to teach or suggest a first latch unit that latches received serial data in response to the first through n-th non-overlapped clock signals of different respective phases that are generated in response to the received clock signal, at least one of the first through n-th non-overlapped clock signals being "in phase with the received clock signal," as claimed.

With regard to the rejection of independent claim 23, it is submitted that the combination of Suemura and Co fails to teach or suggest the present invention as claimed. In particular, the combination of Suemura and Co fails to teach or suggest a method of restoring information data that comprises generating first through n-th non-overlapped clock signals, wherein each clock signal has a predetermined offset and a different respective phase to prevent mutual overlapping, on the basis of a clock signal received via a transmission channel. In Suemura, non-overlapping clock signals are not generated. In Co, the multiple-phase clock signals of Fig. 4 (element 32 of Fig. 3 of Suemura) are generated by a phase locked loop in response to the output of a 32 MHz external crystal oscillator, and not in response to a clock signal received on a transmission channel. In addition, the combination of Suemura and Co fails to teach or suggest at least one of the first through n-th non-overlapped clock signals being "in phase with the received clock signal," as claimed.

Accordingly, it is submitted that Suemura and Co, taken alone or in combination, fail to teach or suggest the invention set forth in independent claims 1, 19 , and 23. Since neither the

Suemura reference nor the Co reference individually teaches or suggests these claimed features, there is no way to combine the references to obtain teaching or suggestion of the claimed features, and, therefore, there is no combination of the references that teaches or suggests the invention as set forth in claims 1, 19, and 23. Accordingly, reconsideration and removal of the rejection of claims 1, 6, 8-9, 19-20, and 23 under 35 U.S.C. 103(a) based on Suemura and Co are respectfully requested.

With regard to dependent claim 2, it is submitted that Sakamoto, like Suemura and Co, fails to teach or suggest fails to teach or suggest the aforementioned features of independent claim 1. Accordingly since Suemura, Co, and Sakamoto, taken alone or in combination, fail to teach or suggest the present invention set forth in the claim, the claims is believed to be allowable over the references. Accordingly, reconsideration of the rejection of claim 2 under 35 U.S.C. 103(a) based on Suemura, Co, and Sakamoto is respectfully requested.

Closing Remarks

Entry of the above amendments and allowance of all claims are respectfully requested. If prosecution of the application can be expedited by a telephone conference, the Examiner is invited to call the undersigned at the number given below.

Respectfully submitted,

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